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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,326	12/15/2003	Thomas J. Goike	05-03-013	3709

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EXAMINER

SIEK, VUTHE

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H.D

Office Action Summary	Application No. 10/736,326	Applicant(s) GOIKE ET AL.	
	Examiner Vuthe Siek	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-7,9-14 and 16-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-7,9-14 and 16-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/736,326 and amendment filed on 11/28/2005. Claims 2-7, 9-14 and 16-20 remain pending in the application, where claims 1, 8 and 15 are canceled.
2. The indicated allowability of claims 2, 6, 7, 9, 13, 14, 16, 20 and 21 are withdrawn in view of the newly discovered reference(s) to Lin et al. (6,980,211 B2). Rejections based on the newly cited reference(s) follow.

Claim Objections

3. Claims 2, 5, 6, 7, 14 and 21 are objected to because of the following informalities: for example in claim 2, line 9, "circuit competent placement" should be changed to --circuit component placement--, to correct spelling. Same objection applies to claims 5-7, 14 and 21. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (6,980,211 B2).

6. As to claims 2 and 5, Lin et al. teach an automatic schematic diagram generation using topology information (a netlist data format) (see abstract, summary, mainly Fig. 5-8, specifically description of Fig. 5). The method for generating an electrical schematic comprising loading a circuit-requirement file (a netlist file, first format; load and save module in Fig. 5), where the netlist file comprises information of component position, component size, component type, connection lines, pin types (Fixed and floating), routing data and generating a schematic definition file as shown in Figs. 6-11, where the schematic file is in a certain format (second format) (see Fig. 5, schematic editing program). Each of component comprises attributes (position, size, type, number of pins) corresponding to a component rule set for selecting and establishing connection lines according to relationships to other components defined by a netlist file (relative connectivity) (see description of Fig. 5). Fig. 6 and 8 shows relative placement position of components. Load and save module stored a netlist file and modified netlist according to design changes (Fig. 5, load and save module 220). Different display modes can be used to automatically display schematic definition file (Fig. 5, display 20, 240). Fig. 6 is in a topology display mode of a schematic definition file where connection lines are shown; Fig. 7 shows normal display mode where there are no connection lines; and Fig. 8 is in abstract display mode showing circuit component placement relationships between components. The generation of schematic is automatically by program setting (col. 9). The generation of schematic is done according to component placement relationships (col. 9-10, a stronger connectivity

relationship). Accordingly, the teachings of Lin et al. clearly anticipated the claim limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 3-4, 6-7, 9-14 and 16-21 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (6,980,211 B2) in view of Hatsch et al. (6,735,742 B2) or Shiitani et al. (6,545,673 B1).

9. As to claims 6-7, 14 and 21, Lin et al. teach all claim limitations as described in rejecting claims 2 and 5. Thus remarks set forth in rejecting claims 2 and 5 is entirely incorporated in rejections of claims 6-7, 14 and 21. Lin et al. teach generating schematic and displaying it on a display unit according to different display modes. The components of a generated schematic have different sizes, shapes and symbols (col. 7, lines 30-39). As shown in Figs. 6-10, components of schematic appeared to have two-dimensional sizes and shapes, except three-dimension. Hatsch et al. teach a three-dimensional arrangement of components in an electronic circuit design taking account of a Z coordinate perpendicular to the X and Y coordinates (col. 6 lines 23-61, col. 7 lines 25-45, col. 8 lines 50-62, col. 9 lines 5-61). The advantage of arrangement of components including two or three-dimensional components is the alteration of the cell

dimensioning should be carried out in such a way that the individual cells of the integrated circuit are modified and placed in such a way that the area is again completely covered by cells, without overlaps occurring. This is done by a program that automatically adapt the heights and widths of the cells, in which case it is possible to prescribe an optimization criterion regarding to minimum height, width and area of the cells (col. 9 lines 5-62). With all these expected results, it would have been obvious to practitioners in the art at the time the invention was made to combine the teachings of Hatsch et al. into generation of schematic as taught by Lin et al. because a new arrangement of components placement can be automatically adapted according to add or delete or change size or shapes of components without any overlapping violation or gap violation.

10. As to claim 3, Lin et al. displaying an electrical schematic corresponding to the schematic output file (Fig. 6 shows displaying a schematic in topology display mode; Fig. 7 shows displaying a schematic in normal display mode; and Fig. 7 shows display a schematic in abstract mode).

11. As to claim 4, Fig. 3 describes schematic editing program 200 operable by a user (col. 7 line 67 to col. 8 line 67).

12. As to claims 9 and 16, Fig. 3 describes load and save module 220, schematic editing program 200 and a netlist file 214. The netlist file is in textual file format and the schematic file is textual and symbolic file format.

13. As to claims 10 and 17, Fig. 3 describes display module 20 and 240 for displaying a schematic corresponding to a schematic output file.

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14. As to claims 11 and 18, Fig. 3 describes a schematic editing program 200 operable by a user automatically (col. 9 lines 1-64).
15. As to claims 12 and 19, Fig. 3 describes a schematic editing program to place components according to component relationships (Fig. 8) and automatically route according to connection lines defined by a netlist file.
16. As to claims 13 and 20, the combination of teachings of Lin (two-dimensional components) and Hatsch (three-dimensional components) would display a mixed combination of two-dimensional and three-dimensional images of components placement corresponding to a generated schematic according to component relationships (See rejection claim 6-7, 14 and 21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



**VUTHE SIEK
PRIMARY EXAMINER**